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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,061	12/27/2000	William P. Hann	062891.0400	8999
7590	04/21/2004			EXAMINER PHAN, TRI H
Bradley P. Williams, Esq. Baker Botts L.L.P. 2001 Ross Avenue Dallas, TX 75201-2980			ART UNIT 2661	PAPER NUMBER
DATE MAILED: 04/21/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/751,061	HANN ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Tri H. Phan	2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE \_\_\_\_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is **FINAL**.                                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 27 is/are allowed.
- 6) Claim(s) 1-7, 10-14 and 17-25 is/are rejected.
- 7) Claim(s) 8,9,15,16 and 26 is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: ____.

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 1, 4-5 and 7 objected to because of the following informalities:
  - In Claim 1, Line 8, "the ATM switch" should be correct to -- an ATM switch -- for clarity.
  - In Claim 4, Lines 2-3, "the ATM card" and "the DSL line card" should be correct to -- an ATM card --and -- a DSL line card -- for clarity.
  - In Claim 5, Line 3, "the ATM card" should be correct to -- an ATM card -- for clarity.
  - In Claim 7, Line 3, "the ATM device" should be correct to -- an ATM device -- for clarity.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
3. Claims 11, 18, 23-24 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- Regarding claim 11, lines 3 and 4, the recitations “the device” are vague and indefinite because it is unclear whether the limitations refer to “the UTOPIA slave device” or “the ATM device”.

- In regard to claim 18, the recitations “devices” (in line 4) and “device” (in line 5) are vague and indefinite because it is unclear whether the limitations refer to “the UTOPIA slave device” or “the UTOPIA master device”.

- Regarding claim 23, line 5, the recitation “plurality of devices” is vague and indefinite because it is unclear whether the limitation refers to “the UTOPIA master device” or “the UTOPIA slave device”. Examiner interprets the claim language as referring to --- plurality of modems --- for the purpose of further examination on the merits.

- In regard to claim 24, line 5, the recitation “plurality of devices” is vague and indefinite because it is unclear whether the limitation refers to “the UTOPIA master device” or “the UTOPIA slave device”. Examiner interprets the claim language as referring to --- plurality of modems --- for the purpose of further examination on the merits.

- Regarding claim 26, line 5, the recitation “associated devices” is vague and indefinite because it is unclear whether the limitation refers to “the UTOPIA master device” or “the UTOPIA slave device”. Examiner interprets the claim language as referring to --- associated modems --- for the purpose of further examination on the merits.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-7, 10-14 and 17-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Nichols et al.** (U.S.6,356,557).

- In regard to claims 1, 7 and 20, **Nichols** discloses in Figs. 3A-B and in the respective portions of the specification about the inter-board communication system and method for passing of high speed Asynchronous Transfer Mode ‘ATM’ data over the standardized Universal Test and Operations Physical Interface for ATM ‘UTOPIA’ bus; wherein the ATM layer device (“*master UTOPIA device*”; For example see Figs. 1 and 3A-B) has the enable register 70 with the data/start-of-cell SOC buffer 80 (“*receive transfer controller*”; For example see Fig. 3B) for controlling the ATM layer’s reception data from the physical devices and the enable register 70 with the data/start-of-cell SOC register 72 (“*transmit transfer controller*”; For example see Fig. 3A) for controlling the transmission data from the ATM layer to the physical devices in the physical layer via connector 53 (For example see Fig. 3A; col. 3, line 3 through col. 5, line 33); the physical layer device (“*slave UTOPIA device*”) has the address remapper 82 with the mux 92 and register 88 (“*receive poll controller*”; For example see Fig. 3B) for determining which

physical devices are ready to receiving or having data registered in the register 88 (“*memory area*”; For example see 3A-B), sending the cell available signal to the ATM layer and receiving the enable signal from the ATM layer (“*communicating the result to the receive transfer controller*”) for receiving data from the data register 72 in the physical layer to the data buffer 80 in the ATM layer (For example see Fig. 3B; col. 5, line 34-57); and has the address remapper 82 with the mux 92 and register 88 (“*transmit poll controller*”; For example see Fig. 3A) for determining which physical devices are ready to transmitting or having transmitting data registered in the register 88 (“*memory area*”; For example see 3A-B), sending the cell available signal to the ATM layer and receiving the enable signal from the ATM layer (“*communicating the result to the transmit transfer controller*”) for transmitting data from the data register 72 in the ATM layer to the data buffer 80 in the physical layer (For example see Fig. 3A; col. 3, line 3 through col. 5, line 33). **Nichols** fails to specifically define about the “*controller*” or “*poll controller*”; however, for “*receive transfer controller*”, the enable register 70 with the data/start-of-cell SOC buffer 80 do control the ATM layer’s reception data from the physical devices, for “*transmit transfer controller*”, the enable register 70 with the data/start-of-cell SOC register 72 do control the transmission data from the ATM layer to the physical devices in the physical layer, for “*receive poll controller*”, the address remapper 82 with the mux 92 and register 88 do determine which physical devices are ready to receiving or having data registered in the register 88, and for “*transmit poll controller*”, the address remapper 82 with the mux 92 and register 88 do determine which physical devices are ready to transmitting or having transmitting data registered in the register 88. Therefore, a person of ordinary skill in the art at the time the invention was made would have recognized that the enable register 70 with the data/start-of-cell

SOC buffer 80 in Fig. 3B as for the “*receive transfer controller*”, the enable register 70 with the data/start-of-cell SOC register 72 in Fig. 3A as for the “*transmit transfer controller*”, the address remapper 82 with the mux 92 and register 88 in Fig. 3B as for the “*receive poll controller*”, and the address remapper 82 with the mux 92 and register 88 in Fig. 3A as for the “*transmit poll controller*”.

- Regarding claims 2-6, **Nichols** further discloses about the clock buffer 74, 79 for receiving the clock signal from the ATM layer in transmitting data (For example see Fig. 3A) and for transmitting the clock signal to the ATM layer in receiving data (For example see Fig. 3B) as in claimed invention 6; and by using polling address incorporating with the cell available and enable signals, the physical layer is “*devoid of*” any memory areas to store the transferring data as in claimed invention 5; and the inter-board connections, e.g. backplane applications, for the ATM layer board (“*ATM card*”; For example see col. 3, lines 62-65) with physical layer boards (“*backplane*” connecting the ATM layer device to the physical devices; For example see col. 5, line 31-59), but fails to explicitly disclose about the “*DSL line card*” as in claimed inventions 3 and 4. However, it is obvious that the physical layer boards can be the “*DSL line card*”, where the application is used for the DSL system as system application choices.

- In regard to claims 10 and 12-13, **Nichols** does disclose about the physical devices connecting with the physical layers and, due to the polling address (“*operable to poll*”), a cell available signal is provided to the register via the physical device, when it is ready to receive or transmit cell (“*available to transfer or receive data*”; For example see col. 3, lines 46-55), but

fails to explicitly disclose about the DSL modems. However, it is obvious that the physical devices, which connect to the physical layer boards, can be the “*DSL modem*”, where the application is used for the DSL system as system application choices.

- Regarding claim 11, **Nichols** further discloses about the mux 92 and demux 94 for multiplexing/demultiplexing data from parallel into serial format, or vice versa (For example see Figs. 3A-B).

- In regard to claim 14, **Nichols** discloses in Figs. 3A-B and in the respective portions of the specification about the inter-board communication system and method for passing of high speed Asynchronous Transfer Mode ‘ATM’ data over the standardized Universal Test and Operations Physical Interface for ATM ‘UTOPIA’ bus; wherein the ATM layer device (“*master UTOPIA device*”; For example see Figs. 1 and 3A-B) has the enable register 70 with the data/start-of-cell SOC buffer 80 (“*receive transfer controller*”; For example see Fig. 3B) for controlling the ATM layer’s reception data from the physical devices and the enable register 70 with the data/start-of-cell SOC register 72 (“*transmit transfer controller*”; For example see Fig. 3A) for controlling the transmission data from the ATM layer to the physical devices in the physical layer via connector 53 (For example see Fig. 3A; col. 3, line 3 through col. 5, line 33); and where the physical layer device (“*slave UTOPIA device*”) has the address remapper 82 with the mux 92 and register 88 (“*receive poll controller*”; For example see Fig. 3B) for determining which physical devices are ready to receiving or having data registered in the register 88, sending the cell available signal to the ATM layer and receiving the enable signal from the ATM layer

(“*communicating to the receive poll controller*”) for receiving data from the data register 72 in the physical layer to the data buffer 80 in the ATM layer (For example see Fig. 3B; col. 5, line 34-57); and has the address remapper 82 with the mux 92 and register 88 (“*transmit poll controller*”; For example see Fig. 3A) for determining which physical devices are ready to transmitting or having transmitting data registered in the register 88 (“*memory area*”; For example see 3A-B), sending the cell available signal to the ATM layer and receiving the enable signal from the ATM layer (“*communicating to the transmit poll controller*”) for transmitting data from the data register 72 in the ATM layer to the data buffer 80 in the physical layer (For example see Fig. 3A; col. 3, line 3 through col. 5, line 33). **Nichols** fails to specifically define about the “*controller*” or “*poll controller*”; however, for “*receive transfer controller*”, the enable register 70 with the data/start-of-cell SOC buffer 80 do control the ATM layer’s reception data from the physical devices, for “*transmit transfer controller*”, the enable register 70 with the data/start-of-cell SOC register 72 do control the transmission data from the ATM layer to the physical devices in the physical layer, for “*receive poll controller*”, the address remapper 82 with the mux 92 and register 88 do determine which physical devices are ready to receiving or having data registered in the register 88, and for “*transmit poll controller*”, the address remapper 82 with the mux 92 and register 88 do determine which physical devices are ready to transmitting or having transmitting data registered in the register 88. Therefore, a person of ordinary skill in the art at the time the invention was made would have recognized that the enable register 70 with the data/start-of-cell SOC buffer 80 in Fig. 3B as for the “*receive transfer controller*”, the enable register 70 with the data/start-of-cell SOC register 72 in Fig. 3A as for the “*transmit transfer controller*”, the address remapper 82 with the mux 92 and register 88 in Fig. 3B as for the

“receive poll controller”, and the address remapper 82 with the mux 92 and register 88 in Fig. 3A as for the “transmit poll controller”.

- Regarding claims 17-18, **Nichols** further discloses about the polling address received by the address remapper (“poll enable signal”; For example see col. 4, lines 43-47; col. 5, lines 23-28), when the appropriate physical device is ready to receive or transmit cells due to the cell available signal via the register to/from the ATM layer device (“receive/transmit transfer controller”; For example see col. 3, lines 46-55).

- Regarding claims 19 and 25, **Nichols** further discloses about the clocks signal due to the polling address of the physical devices in the selection polling cycle and the timing of the clock buffers 74 and 79 in transmitting and receiving data at the ATM layer (“enable/return clocks signal”; For example see Figs. 3A-B, 4A-B, 5A-B; col. 4, line 18-21; col. 5, lines 24-28).

- In regard to claims 21-24, **Nichols** does disclose about the physical devices connecting with the physical layers and, due to the polling address from the ATM layer (“poll enable signal”), a cell available signal is provided from the register (“receive poll controller”) to the ATM layer device, when the physical devices of the physical layer boards (“slave UTOPIA devices”) is ready to transmit cell (“ready to transfer data to master UTOPIA device”; For example see col. 3, lines 46-55), but fails to explicitly disclose about the physical devices are “modems”. However, it is obvious that the physical devices, which connect to the physical layer

boards, can be “*modems*”, where the application is used as system application choices in communication.

***Allowable Subject Matter***

6. Claims 8-9 and 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
7. Claim 26 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.
8. Claim 27 is allowed. The following is an examiner’s statement of reasons for allowance:

Substantially regarding claim 27, the prior art of record fails to disclose the system for communicating data between the master UTOPIA device and the slave UTOPIA device, which comprises the transmit control means for controlling transmission of data from the master UTOPIA device to the slave UTOPIA device, the receive control means for controlling reception of data at the master UTOPIA device from the slave UTOPIA device, the transmit poll means for determining whether the slave UTOPIA device is ready to receive data transmitted by the master UTOPIA device and for communicating the result of the determination to the transmit control means, the receive poll means for determining whether the slave UTOPIA device is ready to

transmit data for reception by the master UTOPIA device and for communicating the result of the determination to the receive control means, the cable means disposed between and connecting together the master UTOPIA device and the slave UTOPIA device and wherein the transmit control means and receive control means are separated from the transmit poll means and the receive poll means by the cable means.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

### *Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

**Cam et al.** (U.S.6,671,758), **Chung et al.** (U.S.6,487,203), **Ganor et al.** (U.S.6,574,228), and **Mizukoshi et al.** (U.S.6,307,858) are all cited to show devices and methods for improving the communication architectures between the ATM layer and the physical layer, which are considered pertinent to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tri H. Phan, whose telephone number is (703) 305-7444. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W. Olms can be reached on (703) 305-4703.

**Any response to this action should be mailed to:**

**Commissioner of Patents and Trademarks**  
Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 305-3900.



Tri H. Phan  
April 5, 2004



D. W. OLMS  
PRIMARY EXAMINER